Serial Link Interface

This document outlines the interface details of a circuit which implements the protocol of a local serial link. The circuit consists of a fiber optic transmitter/receiver pair, the control circuitry, and a delay line. The control circuitry handles both the receiver and transmitter functions. On one end, this circuitry resides on the Digital I/O Transition Module. It communicates with the companion circuitry that resides on the Power Supply Regulator Module.

1.0 Introduction

The Waveform Generator interfaces to the power supplies via a Digital I/O Transition module located at the rear of the VME chassis. The Digital I/O Transition Module communicates with the power supply via a pair of low cost serial fiber optic links. The ADC and DAC are provided as part of the power supply regulator. One link outputs a reference frame to the power supply and the other returns a loopback of the reference frame and readback information from the power supply to the Waveform Generator. The serial links use a bi-phase mark bit stream with a 10Mbit per second bit rate.

The Digital I/O Transition Module will send only one frame,a setpoint, to the power supply synchronous with the 720 Hz RHIC Timeline Event or at a programmable rate of 1, 5, or 10KHz. In return, the power supply will send back, over a separate link, four frames : setpoint loopback, measured I,measured V and measured I dot.

2.0 Frame Format

A fixed length frame of 43 bits is used for the Digital I/O Transition Module Output. When frames are not transmitted, the idle state of the link is a continuous stream of ones. Each frame consists of the following bits and fields:

Start bit (zero)
8-bit type field
24-bit data field
8-bit crc error check ($x^8+x^7+x^5+x^4+x+1$ generating polynomial, excluding start/stop bits)
2- Stop bits (ones)

All signals described in this document are defined as TTL Logic 1 = +5V.

2.0.1 Digital I/O Transition Module Transmission

2.0.1.1 Type Field

The bit pattern defined here guarantees that a frame with a single bit error in the type field will not be misinterpreted as the wrong frame.

setpoint Programmed I 85 (01010101)

2.0.1.2 Data Field

The setpoint field uses all 24 bits in the data field. The data within this field is left justified 2's complement.

bit 23 sign bit
bit 22 msb data
bits 21-1 data
bit 0 lsb data

2.0.2 Power Supply Transmission

For each reception of a setpoint frame, the power supply will respond with the following frames:

Setpoint Loopback
Measured I
Measured V
Measured I dot (Main Magnet System Only)

2.0.2.1 Type Field

Setpoint Loopback	85 (01010101)
Readback Measured I	192 (11000000)
Readback Measured V	193 (11000001)
Readback Measured I dot	194 (11000010)

The two most significant bits of the TYPE field encode the different frame types:

setpoint	01
readbacks	11
undefined	00

The two least significant bits encode the channel number information of the readback. This uniquely defines each of the readback frames for use by the Waveform Generator.

2.0.2.2 Data Field

Readback information is available on a muxed data bus. Address lines A1 and A0 control which data is available on the bus.

Readback data use all 24 bits in the data field. The data within this field shall be left justified 2's complement. The Readbacks- measured I, measured V, and measured I dot- from the power supply shall define the bits as follows:

bit 23 sign
bit 22 msb
bit 21-1 data
bit 0 lsb

3.0 Interface requirements

3.1 Power Supply Interface

3.1.1 Setpoint Updating

The Serial Link Chipset provides the following signals and control lines to the Power supply for setpoint updating:(See Section 4.2.1)

Setpoint Data (24)
Load (1)
Valid (1)

3.1.2 Readbacks

The Power Supply shall provide readback information multiplexed onto a single 24-bit data bus. The Serial Link Chipset will provide two signal lines which encode the channel that is available on the bus.

Readback (24)
Address (2)
Measured I 00
Measured V 01
Measured I dot 10

3.2 Waveform Generator Interface

3.2.1 Setpoint Loading (See Section 4.1.1)

Setpoint (24)
Setpoint Load (1)
Trigger Xmit (1)

3.2.2 Readbacks provided to the Waveform Generator (See Section 4.1.2)

Type Field (4)
Data Field (24)
Data Valid (1)
Frame Error (1)

4.0 Functionality

4.1 Transition Module

4.1.1 Transmission

One 24 bit register will be provided for use by the Waveform Generator Moduleand is called the SETPOINT register. An active low LOAD pulse, SETPTLD, is necessary to latch the data into the register on the rising edge. In addition, the transmission of the setpoint frame will occur when a TRIGXMIT pulse has been received from the Waveform Generator Module. The Type field will be hard coded.

4.1.2 Reception

Readback frames from the power supply will be provided via a 4-bit type field register and a 24-bit data field register. Upon successful decoding of a valid frame from the power supply, a DATA VALID will be issued. Loopback information will also be provided via these same two registers. In addition, a FRAME ERROR signal will be provided.

4.2 Power Supply

4.2.1 Reception

Each frame received by the power supply will contain an 8-bit type field and a 24-bit data field. A LOAD pulse will be generated when it has been determined that the received frame has the correct header and trailer information, as well as the correct number of bits. This pulse will be issued regardless of the internal data integrity. A VALID pulse will be generated when a frame has been received with no errors. On the occurrence of both the LOAD and VALID pulses, the 24-bit setpoint can be latched.

4.2.2 Transmission

Loopback of the setpoint will be accomplished by providing the decoded serial bit stream directly to the encoder section of the transmitter. In this way, the data will be sent back exactly as received without calculating a new crc checkwork. In addition, this data will be checked for errors and made available to the power supply. Upon completion of the loopback function, the readbacks will be loaded in succession and transmitted to the Waveform Generator Module.

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